ABSTRACT

An integrated circuit (IC) chip, mounted on a leadframe, has a network of power distribution lines deposited on the surface of the chip so that these lines are located over active components of the IC, connected vertically by metal-filled vias to selected active components below the lines, and also by conductors to segments of the leadframe.

The network relocates most of the conventional power distribution interconnections from the circuit level to the newly created surface network, thus saving substantial amounts of silicon real estate and permitting shrinkage of the IC area.

The network is electrically connected to selected active components by metal-filled vias; since these vias can easily be redesigned to other locations, IC designers gain a new degree of design freedom.

The network relocates most of the bond pads dedicated to power supply from the conventional alignment along the chip periphery onto the newly created bondable lines, saving substantial additional amounts of silicon real estate, and freeing the bonding machines from their extremely tight connector placement and attachment rules to much more relaxed bonding programs.

The network is deposited and patterned in wafer processing as a sequence of metal layers specifically suited for providing power current and electrical ground potential. The network has attachable outermost metal surface and is laid out so that network portions form pads convenient for attaching balls of bonding wires or solder.